L Number	Hits	Search Text	DB	Time stamp
1	42385	ccd	USPAT; US-PGPUB	2002/07/29 07:47
2	408	"oxide-nitride"	USPAT; US-PGPUB	2002/07/29 07:48
3	13	"oxide-nitride" and ccd	USPAT; US-PGPUB	2002/07/29 07:58
4	5171	"gate dielectric"	USPAT; US-PGPUB	2002/07/29 07:59
5	23569	oxide near2 nitride	USPAT; US-PGPUB	2002/07/29 07:59
6	289	"gate dielectric" with (oxide near2 nitride)	USPAT; US-PGPUB	2002/07/29 07:59
7	0	ccd with ("gate dielectric" with (oxide near2 nitride))	USPAT; US-PGPUB	2002/07/29 08:00
8	123	ccd and "gate dielectric"	USPAT; US-PGPUB	2002/07/29 08:00
9	84272	nitride	USPAT; US-PGPUB	2002/07/29 08:00
10	71	(ccd and "gate dielectric") and nitride	USPAT; US-PGPUB	2002/07/29 08:00
11	201472	@ad>20000626 or @rlad>20000626	USPAT; US-PGPUB	2002/07/29 08:01
12	65	((ccd and "gate dielectric") and nitride) not (@ad>20000626 or @rlad>20000626)	USPAT; US-PGPUB	2002/07/29 08:01

EAST Browser - L3: (13) 2 and 1 | US-4047215-A | Tag: 5 | Doc: 13/13 (SORTED) | Format : KWIC

File Edit View Tools Window Help

I.E.E.E., June, 1972, pp. 721 and 722 "A Uniphase Charge Coupled Device," suggest a structure making use of charge storage in an MNOS (metal nitride oxide silicon) structure to define in the silicon substrate the asymmetric potential wells required for unidirectional charge flow. The structure includes a silicon substrate with overlying layers of silicon dioxide and silicon nitride and spaced apart individual charge transfer electrodes on the nitride layer. Required potential wells are defined by forming an appropriate pattern of charge accumulation at the oxide-nitride interface. R. D. Melen and James D. Meindl, I.E.E.E., Journal of Solid State Circuits, February, 1972, pp. 92-93 propose a two-phase CCD structure employing a two-level offset aluminum-polysilicon gate structure with the aluminum and polysilicon gates connected together in pairs. Alternate gate pairs are connected to respective clock lines, one of which is held at a d.c. bias while clock pulses are applied to the other clock line. Both of these proposals have inherent fabrication and/or functional disadvantages.

Brief Summary Text - BSTX:

It is an object of the present invention to provide a uniphase CCD structure having a relatively simple structure and manner of operation.

Brief Summary Text - BSTX:

According to the present invention, a uniphase charge coupled device structure

Details | Text | Image | HTML | KWIC

There have previously been reported proposals for CCDs using only a single clock signal. P. P. Gelberger and C. A. T. Salama, Proceedings of the I.E.E.E., June, 1972, pp. 721 and 722 "A Uniphase Charge Coupled Device," suggest a structure making use of charge storage in an MNOS (metal nitride oxide silicon) structure to define in the silicon substrate the asymmetric potential wells required for unidirectional charge flow. The structure includes a silicon substrate with overlying layers of silicon dioxide and silicon nitride and spaced apart individual charge transfer electrodes on the nitride layer. Required potential wells are defined by forming an appropriate pattern of charge accumulation at the oxide-nitride interface. R. D. Melen and James D. Meindl, I.E.E.E., Journal of Solid State Circuits, February, 1972, pp. 92-93 propose a two-phase CCD structure employing a two-level offset aluminum-polysilicon gate structure with the aluminum and polysilicon gates connected together in pairs. Alternate gate pairs are connected to respective clock lines, one of which is held at a d.c. bias while clock pulses are applied to the other clock line. Both of these proposals have inherent fabrication and/or functional disadvantages.

Brief Summary Text - BSTX:

It is an object of the present invention to provide a uniphase CCD structure having a relatively simple structure and manner of operation.

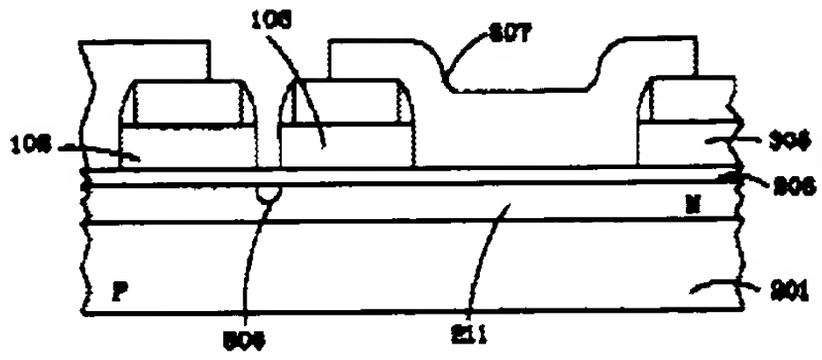


FIG. 3c

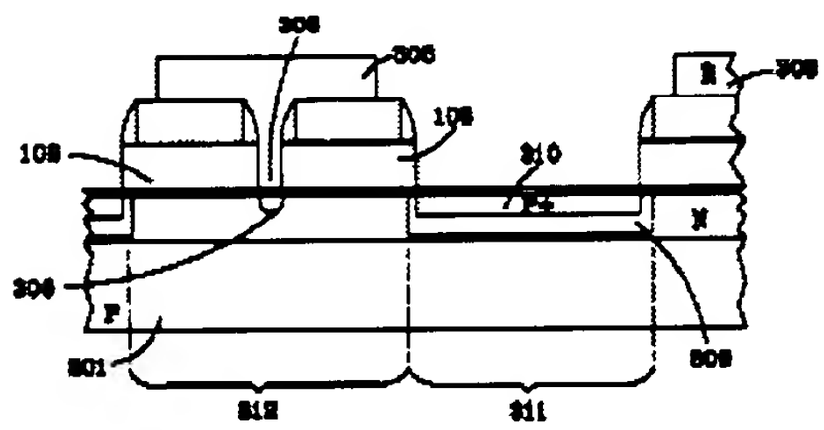


FIG. 3d

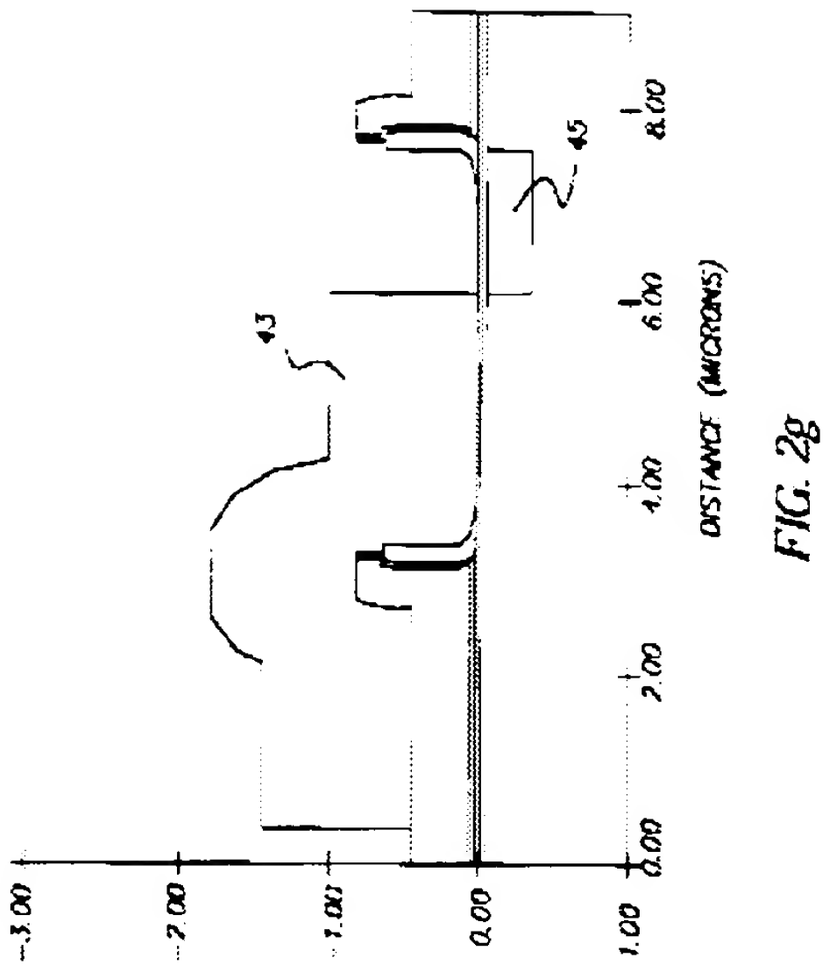


FIG. 2g

US-PAT-NO: 6051852

DOCUMENT-IDENTIFIER: US 6051852 A

TITLE: Self aligned LOD antiblooming structure for solid-state imagers

---------- KWIC ---------

It is the object of this invention to solve the above mentioned problems with the prior art. This invention discloses a process for providing a self-aligned, LOD antiblooming structure whose antiblooming barrier height can be set by process (via implantation), and is relatively insensitive to process variations. An extra gate electrode to set the antiblooming barrier height is not required (as with some other disclosures), but may be provided so as to allow for electronic exposure control to use with FT image sensors. The antiblooming overflow channel length is determined photolithographically and is therefore, easily adjusted by layout. The process is simple and compatible with different types of gate dielectrics such as O (Si0.sub.2), ON (oxide nitride), or ONO (oxide nitride oxide).

US-PAT-NO: 5536678

DOCUMENT-IDENTIFIER: US 5536678 A

TITLE: Method of manufacturing a wiring arrangement for a semiconductor device using insulating and etch stop layers

--------- KWIC ---------

The device comprises a semiconductor body 10 of silicon with a surface 11 at which or near which the charge-coupled device 12 and the MOS transistor 13 are situated. The charge-coupled device comprises a range of clock electrodes 3a, 3b, 3c, etc. formed by thin, approximately 50 nm thick polycrystalline silicon tracks. These clock electrodes 3 constitute the conductive regions referred to above and are separated from the surface 11 by the thin dielectric layer 14. In the present embodiment, the gate dielectric only comprises a silicon oxide layer, but it may obviously also consist of a different insulating material or of double layers of, for example, silicon oxide and silicon nitride . The clock electrodes 3 are embedded in a dielectric layer 15 which may be entirely of silicon oxide, but which may obviously also be composed entirely or partly of other materials. The layer 15 is composed of two portions 15a and 15b, which will be discussed below.

US005516716A

United States Patent [19]

Hawkins et al.

[11] Patent Number: 5,516,716

[45] Date of Patent: May 14, 1996

[54] METHOD OF MAKING A CHARGE COUPLED DEVICE WITH EDGE ALIGNED IMPLANTS AND ELECTRODES

[75] Inventors: Gilbert A. Hawkins, Mendon; David L. Losee, Fairport, both of N.Y.

[73] Assignee: Eastman Kodak Company, Rochester, N.Y.

[21] Appl. No.: 349,120

[22] Filed: Dec. 2, 1994

[51] Int. Cl.[6] H01L 21/339
[52] U.S. Cl. 437/53; 437/26; 437/984
[58] Field of Search ..... 437/28, 53, 52, 437/984; 148/DIG. 53, DIG. 111

[56] References Cited

U.S. PATENT DOCUMENTS

[illegible]	[illegible]	Kahng et al.	357/24
[illegible]	[illegible]	Kahng	357/24
[illegible]	[illegible]	Krambeck et al.	[illegible]
[illegible]	[illegible]	Amelio et al.	[illegible]
[illegible]	[illegible]	Anthony et al.	[illegible]
[illegible]	[illegible]	Tasch et al.	[illegible]
[illegible]	[illegible]	Frye et al.	[illegible]
[illegible]	[illegible]	Tasch, Jr. et al.	[illegible]
[illegible]	[illegible]	Hynecek	[illegible]
[illegible]	[illegible]	Losee et al.	[illegible]
[illegible]	[illegible]	Hawkins et al.	[illegible]
[illegible]	[illegible]	Chow et al.	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	Cox et al.	[illegible]
[illegible]	[illegible]	Nichols et al.	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]	[illegible]	Japan	[illegible]

OTHER PUBLICATIONS

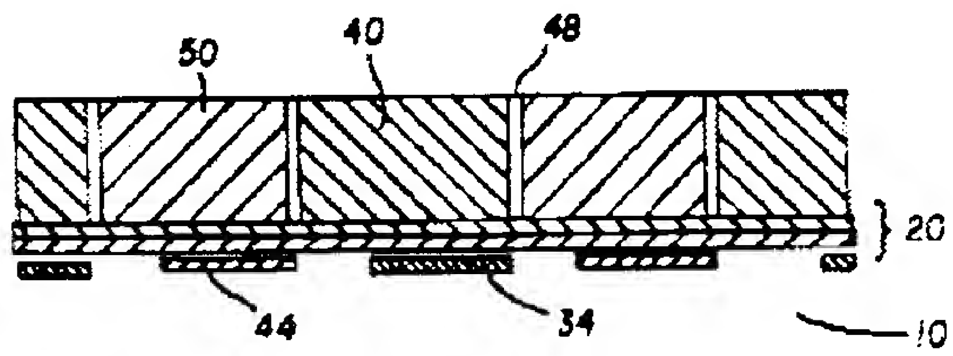
Banghart et al., Charge Transfer in the Presence of Potential Barriers, COMPEL—The International Journal for Computation and Mathematics in Electrical and Electronic Eng., vol. 10, No. 4, pp. 205–213, Dec. 1991.

Primary Examiner—Charles Chaudhari?
Attorney, Agent, or Firm—Raymond L. Owens

[57] ABSTRACT

A fully self-aligned, charge coupled device (CCD) comprises a semiconductor substrate having implanted barrier and/or storage regions, an insulating dielectric layer disposed over the substrate, a first layer of closely spaced electrodes in self-alignment with at least one implant underneath the first electrodes, a second layer of closely spaced electrodes in self-alignment with the first electrodes and with at least one implant underneath the second electrodes also in self-alignment with the first electrodes. The process for fabricating the fully self-aligned CCD comprises the steps of first forming upon the semiconductor substrate, a uniform insulating dielectric layer, then forming a sacrificial layer upon the dielectric layer, the sacrificial layer patterned by removal of selected portions of the layer, at least one edge of the patterned sacrificial layer serving as a mask for ion implantation into the semiconductor substrate, the mask optionally comprising also photoresist; then forming in only those regions in which the sacrificial layer was removed, a first gate electrode; then removing the sacrificial layer, thereby exposing the sidewalls of the closely spaced first gate electrodes, at least one of the sidewalls serving as a mask for a second ion implantation into the semiconductor substrate, the mask optionally comprising also photoresist; then forming a thin oxide layer over the exposed surface of the first gate electrode; then depositing and patterning a second gate electrode layer to form a second gate electrode disposed between portions of the first gate electrode.

30 Claims, 9 Drawing Sheets



US005460997A

United States Patent [19]

Hawkins et al.

[11] Patent Number: 5,460,997

[45] Date of Patent: Oct. 24, 1995

[54] METHOD OF MAKING A CONFINED PLANAR CHARGE COUPLED DEVICE WITH EDGE ALIGNED IMPLANTS AND INTERCONNECTED ELECTRODES

[75] Inventors: Gilbert A. Hawkins, Mendon; Robert L. Nielsen, Pittsford, both of N.Y.

[73] Assignee: Eastman Kodak Company, Rochester, N.Y.

[21] Appl. No.: 396,504

[22] Filed: Jan. 23, 1995

[51] Int. Cl.[6] H01L 21/339

[52] U.S. Cl. 437/53; 437/60; 148/DIG. 50

[58] Field of Search ..... 437/50, 53, 784; 148/DIG. 50, DIG. 111

[56] References Cited

U.S. PATENT DOCUMENTS

4,766,088 [illegible] Davids et al. 437/53
5,340,??? [illegible] [illegible] 437/53

Primary Examiner—Chandra Chaudhari

Attorney, Agent, or Firm—Raymond L. Owens

[57] ABSTRACT

A method of making a fully self-aligned, planar, two phase charge coupled device comprises the steps of first forming upon a semiconductive substrate a uniform first insulative dielectric layer, then depositing and patterning in the form of a mask according to the first insulative layer a second insulative layer, then implanting ions of a second conductivity type into the substrate, then patterning closely spaced strips of a first conductive layer on the first and second insulative layer, then further implanting ions of a second conductivity type in the regions between said first conductive strips, then depositing uniformly a second conductive layer electrically isolated from the first conductive strips, then entirely removing by uniform planarization those portions of the second conductive layer disposed over regions of the first conductive strips or over segments of the second insulative layer so as to form closely spaced, coplanar, alternating first and second electrically isolated conductive strips, then electrically connecting alternate pairs of strips by a planar process of depositing and oxidizing a conductive material, then removing portions of the second insulative layer.

11 Claims, 13 Drawing Sheets